REMARKS

Examiner T. Phan is thanked for the thorough examination and search of the subject Patent Application. Claims 1, 4, 14, 16, 26, and 27 have been amended.

The drawings have been corrected in red to overcome the objections raised by the Examiner. Fig. 1 has been corrected to remove the non-referenced signs S, D, and CG. Fig. 5 has been corrected to show transistors 46c-46n. Fig. 5 has also been amended to show the connection of the flash EPROM memory cell 52. The Specification has been amended to refer to the flash EPROM memory cell in the drawing figure.

Reconsideration of the rejection of Claims 1-27 under 35 U.S.C. 112 first paragraph is requested in view of amended drawing Fig. 5 and the amended Specification and in accordance with the following remarks.

The connection of the functional and testing circuit to the flash EPROM memory cell is illustrated in the proposed drawing correction to Fig. 5. It is believed that this proposed drawing correction overcomes the rejection a). The value of "n" diode-connected transistors depends on the threshold voltage of the transistors and the breakdown voltage of the diodes. This explanation is believed to overcome rejection b).

Reconsideration of the rejection of Claims 1-27 under 35 U.S.C. 112 first paragraph is requested in view of amended drawing Fig. 5 and the amended Specification and in accordance with the remarks above.

Claims 1, 4, 14, 16, 26, and 27 have been amended to overcome rejection of Claims 1-27 under 35 U.S.C. 112 second paragraph. It is believed that these amendments overcome the indefiniteness rejection.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of the rejection under 35 U.S.C. 102 of Claims 1-27 as being anticipated by Kim is requested in accordance with the following remarks.

Applicants' invention comprises a functional circuit (core circuit) and a testing circuit. Kim provides a method to lower the erase voltage in a functional circuit. Applicants' invention provides a testing method to confirm the endurance of a Flash device by the testing circuit. Kim does not mention testing at all and so has nothing to do with the device, method, and detailed claims of Applicants' invention.

Reconsideration of the rejection under 35 U.S.C. 102 of Claims 1-27 as being anticipated by Kim is requested in accordance with the remarks above.

Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Specification and Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner T. Phan not find that the Claims are now Allowable that the Examiner call the undersigned at 765 4530866 to overcome any problems preventing allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please replace the third paragraph of page 8 with the following:

Refer now to Fig. 5, schematically depicting the method of the present invention. A Flash EPROM cell 52 is to be erased. The cathode of a protective diode 38 is connected to a charge pump circuitry 36. The anode of the protective diode 38 is connected to one (or more) diode-connected NMOS transistor(s) 40, for example. A diode-connected NMOS transistor is one where the drain and gate are connected. When conducting, the voltage drop across each diode-connected NMOS transistor will be equal to the transistor threshold voltage (V_t).

Please replace the first full paragraph of page 9 with the following:

The function of the margin erase circuit of the present invention is now described. During normal operation of the Flash EPROM cell 52, the bypass switch 50 is opened. The voltage, V_E, regulated by this regulator will be the normal erase voltage (V_{NE}), which is the sum of the voltage drops across transistors 46a-46n and 40 and the breakdown voltage (V_{bd}) of the protective diode 38. Since the voltage drop across each transistor 46a-46n and 40 is equal to V_t (threshold voltage of NMOS transistor), the normal erase voltage observed at the cathode of the protective diode 38 is given by:

$$V_{NE} = V_{bd} + V_t + n*V_t .$$

During testing of the Flash EPROM cell 52, the bypass switch 50 is closed thereby bypassing transistors 46a-46n. This reduces the voltage observed at the cathode of the protective diode 38 by $n*V_t$. Thus, the margin erase voltage is given by:

$$V_{ME} = V_{bd} + V_t.$$

IN THE CLAIMS

Please amend the Claims as follows:

1. (AMENDED) A method of margin erasing memory cells in [the] a testing procedure of a flash EPROM memory in an integrated circuit [whereby] wherein said margin erasing uses [the same] charge pump circuitry to develop both [the] a normal erase voltage used by [the] an end user and [the] a margin erase voltage used in said testing procedure.

4. (AMENDED) The method according to Claim 3 [whereby] wherein said series connected voltage dropping components are [selected from the group consisting of:] diode connected NMOS transistors, PMOS transistors, native NMOS transistors [and] or diodes.

14. (AMENDED) A method of margin erasing memory cells in [the] a testing procedure of a flash EPROM memory in an integrated circuit [whereby] wherein said margin erasing uses [the same] an internal charge pump circuit to develop both [the] a normal erase voltage used by [the] an end user and [the] a margin erase voltage used in said testing

procedure and [whereby] wherein said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage.

16.(AMENDED) The method according to Claim 15 [whereby] wherein said series connected voltage dropping components are [selected from the group consisting of:] diode connected NMOS transistors, PMOS transistors, native NMOS transistors [and] or diodes.

26. (AMENDED) A flash EPROM memory device comprising:

a charge pump circuit;

a protective diode having a cathode and an anode [whereby the] wherein said cathode of said protective diode is connected to said charge pump circuit;

a plurality of series connected voltage dropping devices [whereby the] wherein a drain of a first [of two terminals] of said plurality of series connected voltage dropping devices is connected to [the] said anode of said protective diode;

a bias current source connected to [the second of two terminals] a source of a last of said plurality of series connected voltage dropping devices; and

a bypass switch to bypass one or more of said series connected voltage dropping devices.

27. (AMENDED) The method according to Claim 26 [whereby] wherein said series connected voltage dropping devices are [selected from the group consisting of:] diode connected NMOS transistors, PMOS transistors, native NMOS transistors [and] or diodes.